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Ferroelectric Gated Electrical Transport in CdS Nanotetrapods

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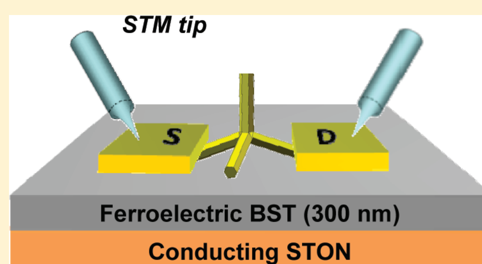
S Supporting Information

ABSTRACT: Complex nanostructures such as branched semiconductor nanotetrapods are promising building blocks for next-generation nanoelectronics. Here we report on the electrical transport properties of individual CdS tetrapods in a field effect transistor (FET) configuration with a ferroelectric $Ba_{0.7}Sr_{0.3}TiO_3$ film as high-*k*, switchable gate dielectric. A cryogenic four-probe scanning tunneling microscopy (STM) is used to probe the electrical transport through individual nanotetrapods at different temperatures. A p-type field effect is observed at room temperature, owing to the enhanced gate capacitance coupling. And the reversible remnant polarization of the ferroelectric gate dielectric leads to a well-defined nonvolatile memory effect. The field effect is shown to originate from the channel tuning in the arm/core/arm junctions of nanotetrapods. At low temperature (8.5 K), the nanotetrapod devices exhibit a ferroelectric-modulated single-electron transistor (SET) behavior. The results illustrate how the characteristics of a ferroelectric such as switchable polarization and high dielectric constant can be exploited to control the functionality of individual three-dimensional nanoarchitectures.



KEYWORDS: Nanotetrapod, ferroelectric, field effect, nonvolatile memory, band alignment, scanning probe microscopy

The continuing miniaturization of electronic devices is approaching its physical and technological limitations.[1] This has inspired extensive efforts to develop alternative bottom-up fabrication of nanoelectronic devices to address the imminent technology demands on the basis of nanostructured materials and motifs.[2−7] Among them, the multiarmed II−VI semiconductor nanotetrapods,[8−21] which normally consist of four wurtzite-structured "arms" projecting out at the tetrahedral angle bridged at a pyramidal shaped zincblende-structured "core", are of particular interest due to their unique nanoscale three-dimensional (3D) architectures that can deliver functionalities of delicate multiterminal nanodevices.[17] As compared to conventional semiconductor nanocrystals such as nanoparticles and nanorods, the branched nanotetrapods possess a peculiar electronic structure and the band alignment at the interface of the zincblende core and the wurtzite arms needs to be taken into account. As revealed by theoretical calculations, CdX (X = S, Se, Te) compounds in a wurtzite phase have a larger band gap than in a zincblende phase,[8] and for the nanotetrapod structures in particular the band offset at the zincblende/wurtzite interface can result in an electron localization in the zincblende core and a hole localization in the wurtzite arms.[9−11,16] Such a type II band alignment is expected to have significant implications in the electrical transport properties of semiconductor nanotetrapods. However, thus far experimental studies on the electrical transport properties in such nanotetrapod structures have been rather limited. A pioneering work in this regard was reported by Cui et al. in 2005, where they studied the electrical transport in CdTe nanotrapods and observed a single-electron transistor (SET) effect at low temperature by using a Si_3N_4 film as gate dielectric.[12]

A technological challenge for experimentally modulating the conductance of the semiconductor nanotetrapods lies in their unique 3D geometric shape that makes the tetrapod structures impossible to lie flat on the planar substrate surfaces and thus seriously hampers the capacitance coupling between the gating electric field and the tetrapod conduction channels. A possible way to overcome this obstacle is to use a gate dielectric layer that has high dielectric constant so as to enhance capacitance coupling in a complementary way. Ferroelectric insulating films, as compared to other widely used high-*k* dielectrics such as Al_2O_3 (∼8), ZrO_2 (∼20), and HfO_2 (∼30),[6,7,22] possess not only even higher dielectric constant (∼100 or higher) but also the characteristic of spontaneous polarization, which presents a promising opportunity for the construction of ferroelectric field effect transistors (FeFETs) with nonvolatile memory functions.[23−27] Actually, 1D nanowire transistors with integrated ferroelectric dielectrics have already been demonstrated to exhibit nonvolatile memory effect.[28−34] More recently, we reported on a well-defined intrinsic

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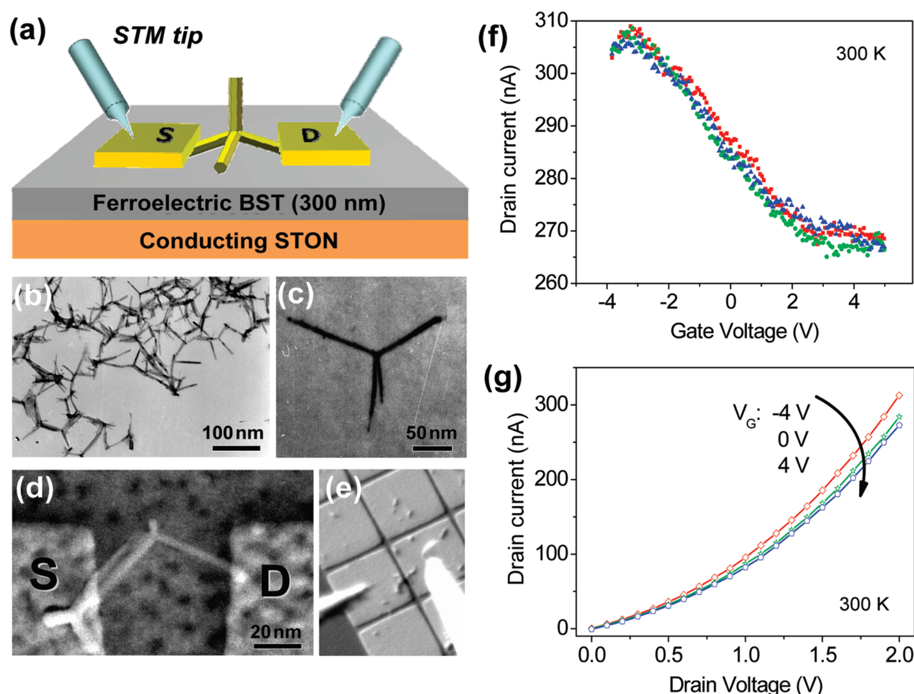

Figure 1. (a) Schematic illustration of a nanotetrapod transistor with a 300 nm-thick ferroelectric dielectric under testing with STM tips. The source (S) and drain (D) electrodes are patterned Pt layer. (b) Typical TEM image of the multiarmed CdS nanorods used in this study. The enlarged micrograph of a single CdS nanotetrapod is shown in (c). (d) SEM image of a single CdS nanotetrapod device. (e) In situ SEM image of two STM tips (in white) probing on a testing device. (f) Typical transfer characteristics ($I-V_G$) of a single CdS nanotetrapod device measured at room temperature. (g) The corresponding $I-V$ curves of the nanotetrapod under gate voltages of −4, 0, and 4 V.

memory switch behavior in the single-walled carbon nanotube-based FeFET.[35,36] Here, we utilize high-*k* ferroelectric $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) as gate dielectric to study the electrical transport in individual CdS nanotetrapods. The electrical transport properties of CdS nanotetrapods are probed using a cryogenic four-probe scanning tunneling microscopy (STM)[37] at different temperatures (Figure 1a). For the first time, an electric field effect is realized in CdS nanotetrapods at room temperature, owing to the enhanced gate capacitance coupling enabled by the BST dielectric. Moreover, ferroelectric memory effects, including a ferroelectric-modulated SET behavior at 8.5 K, are demonstrated by controlling the polarization of the ferroelectric thin film.

The synthesis of the multiarmed CdS nanorods was accomplished through a wet chemical growth approach, which involved the kinetically controlled precipitation of Cd^{2+} with S^{2-} in aqueous solution at a mild temperature of 80 °C, as previously reported.[20,21] The as-grown multiarmed CdS nanorods are commonly a mixture of one-, two-, three-, and four-armed rods, bipods, tripods, and tetrapods, respectively, with the tetrapods dominating. Figure 1b displays a typical transmission electron microscopy (TEM) image of the as-grown samples, and Figure 1c shows an enlarged micrograph of an individual tetrapod. The multiarmed CdS nanorods consist of a tetrahedral zincblende core with epitaxially grown wurtzite arms along the [001] direction. The pod arms normally have lateral diameters of 6−8 nm and lengths of tens of nanometers with some extending over 100 nm. For device fabrication, a 300 nm-thick epitaxial ferroelectric BST film was deposit on a single crystal Nb-doped (001) $SrTiO_3$ (STON) substrate by using pulsed laser deposition (PLD). The PLD was carried out in 30 Pa of O_2 at 800 °C, followed by an in situ post annealing at 600 °C in oxygen ambient of 1 bar for 30 min to neutralize the oxygen vacancy and improve the crystallization of the thin film. Temperature-dependent permittivity shows that the ferroelectric−paraelectric phase transition in such film occurs over a wide temperature range in comparison to the sharp transition of its bulk counterpart at 314 K (see Figure S1, Supporting Information). The multiarmed CdS nanorods were dispersed in ethanol and then deposited onto the ferroelectric substrate through a facile spin-coating process. Electron beam lithography (EBL), Pt deposition, and lift-off procedures were performed for source and drain electrode patterning (Figure 1d). As illustrated schematically in Figure 1a, electrical transport measurements of CdS tetrapod devices were performed in dark in a four-probe STM chamber under ultrahigh vacuum (base pressure <2 × 10^{-10} Torr) at temperature range of 8.5−400 K. STM tips (tungsten) were used to directly probe the source−drain current with an applied back gate voltage. The conductive STON substrate serves as back gate electrode. Dozens of devices were fabricated and tested.

Figure 1f shows the typical current (I) versus gate voltage (V_G) characteristics (with source−drain bias V_{SD} = 2 V) of a nanotetrapod device at room-temperature (300 K). The three overlapped curves are from different measurements on the same device. A p-type field effect behavior can be clearly seen. The percentage of the current change due to electrostatic field modulation can be deduced as $(I_{max} - I_{min})/I_{max} \times 100\%$ = 13%, which is significant if taking into account the vacuum gap between the ferroelectric BST dielectric and the tetrapod junction. The leakage current of the devices is less than 1 nA with a sweeping gate voltage up to 8 V (not shown here). Figure 1g shows the source−drain current versus voltage ($I-V$) curves of the nanotetrapod device under different gate voltages. In order to protect the nanotetrapod devices from electrical damage, here we

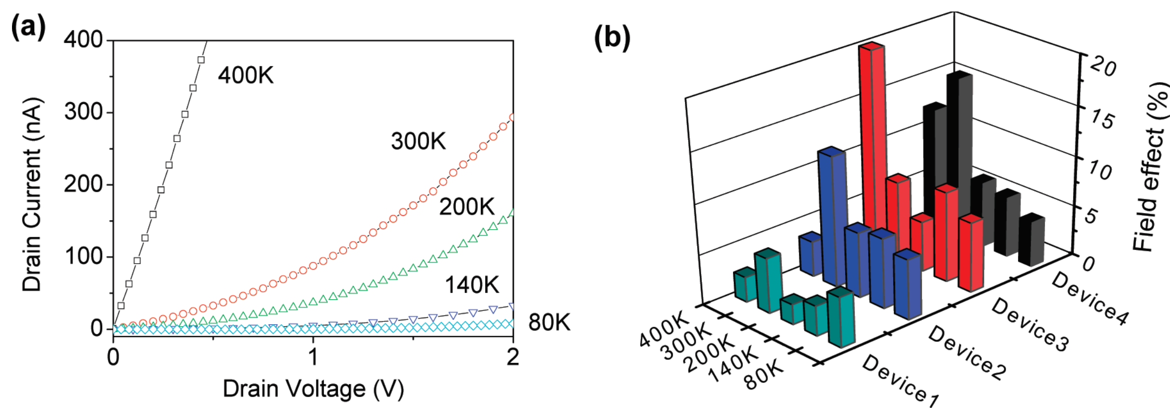

Figure 2. Temperature dependent electrical characteristics of the nanotetrapod device. (a) Typical temperature dependent $I-V$ curves of the nanotetrapod with $V_G = 0$ V, measured at 80, 140, 200, 300, and 400 K, respectively. (b) The magnitudes of the field effect ($(I_{max} - I_{min})/I_{max} \times 100\%$ at ± 4 V) of four different nanotetrapod transistors measured at different temperatures.

constrained our measurement in the unsaturated section. When the gate voltage changes from negative to positive, the current decreases gradually, consistent with the p-type transfer characteristics. It is worth noting that this is the first demonstration of the electric field effect at room temperature in a semiconductor tetrapod nanoarchitecture.

To further examine the field effect, we have measured temperature dependent electrical transport in CdS nanotetrapods. Figure 2a shows $I-V$ curves of the above device measured at 80, 140, 200, 300, and 400 K (at $V_G = 0$ V), respectively. The conductance increases with temperature, showing an activated behavior (with more analysis below). The temperature dependent variations of the field effect measured for four nanotetrapod devices are summarized with a 3D bar plot in Figure 2b. Interestingly, three devices show maximum field effect at 300 K with another peaking at 400 K. This result correlates well with the temperature dependence of the dielectric constant of BST ferroelectric film, which exhibits a diffuse transition peak at around 300 K (see Supporting Information, Figure S1). The enhanced gate capacitance coupling is thus enabled by ferroelectric film in the nanotetrapod devices with comparison to the FET with conventional dielectric SiN_x.[12] At cryogenic temperature of 8.5 K, a Coulomb charging effect is observed in CdS nanotetrapod devices (see Supporting Information, Figure S2), similar to the report on the CdTe nanotetrapods by Cui et al.[12] The addition energy extracted from the height of the Coulomb diamond is around 70 meV, comparable to the value (~30 meV) for CdTe nanotetrapod SET devices.[12] As pointed out by Cui et al., this magnitude of addition energy cannot be accounted by charging the whole nanotetrapod as a single quantum dot, but rather due to the core moiety only.[12]

The use of ferroelectric BST film as gate dielectric enables us to explore the memory function of the CdS nanotetrapod device. The memory effect can be expected by tuning the polarization of ferroelectric thin film using gate voltage sweep.[23−36] We show in Figure 3 the hysteretic loops of the $I-V_G$ transfer characteristics measured at different temperatures. At 300 K, a counter-clockwise hysteresis loop is observed when the gate voltage sweeps upward (from negative to positive) and then downward continuously (Figure 3a). This is different from a ferroelectric memory loop and can be attributed to a "charge-storage" memory effect. In a FET configuration, charge traps such as surface absorbents and defects in dielectric layer can act as floating gates, affecting the charge distribution near the conduction path. Such a "charge-storage" effect can change with the gate voltage and give rise to a memory effect characterized by a counterclockwise hysteresis loop, as widely seen in carbon nanotube transistor memory devices.[4,5] The defect-induced charge−storage effect is more pronounced at high temperature when more charge traps are activated, whereas at low temperature most charge traps are inactive and the charge-storage effect can be largely suppressed. Figure 3c shows the transfer characteristic loops of the same nanotetrapod device measured at 80 K. Now a "clockwise" hysteresis loop is clearly seen when the gate voltage sweeps upward and then downward continuously, a hallmark of ferroelectric memory effect. The threshold voltage (V_{th}, defined as the gate voltage at which $I = 390$ nA) changes from −1 to −3.5 V for the upward and downward voltage sweeps respectively, giving a memory window ΔV_{th} of 2.5 V. The competition between the ferroelectric memory effect and the charge-storage effect gives rise to a midpoint where essentially no hysteresis is seen at 140 K, as shown in Figure 3b. Thus, in CdS nanotetrapod devices, the charge−storage effect plays an important role against the ferroelectric memory effect, especially at higher temperature.

Figure 3d shows the current modulations in the nanotetrapod device as a function of V_G (with $V_{SD} = 50$ mV) at 8.5 K. When V_G sweeps upward from negative to positive and then downward continuously, the two spectra show a 6V negative position shift, as marked by the shaded blocks in Figure 3d. The spectrum shift is associated with the polarization tuning in the BST ferroelectric. That is, when the nanotetrapod is first negatively biased with respect to the metallic STON gate, the polarization in the ferroelectric film will be aligned away from the nanotetrapod. And the resulting negative remnant polarization of the ferroelectric thin film will lift the bands of the core upward, giving rise to a positive shift of the electrical spectra of the nanotetrapod device. Reversely, when sweeping downward, a negative shift of the electrical spectra will be obtained. Here we note that the shapes of $I-V_G$ curve in upward and downward directions are not exactly the same, though each marked segment (in shade) in Figure 3d consists of a high current plateau followed by two low current peaks. This shape change may come from a voltage-tunable dielectric constant of the ferroelectric BST films.[38] If the red circle point, marked in Figure 3d, in the upward sweeping curve represents a high-current binary "1" state of the memory operation, then the circled point in the downward sweeping curve can correspond to a binary "0" state. Thus, a prototype ferroelectric memory is demonstrated at single-electron level.[39,40]

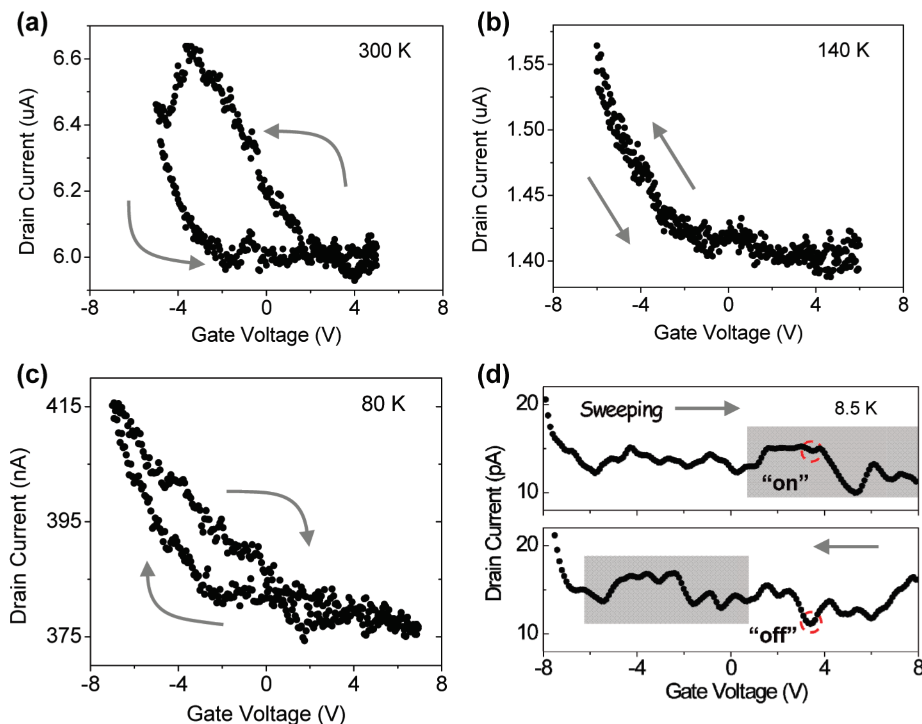

Figure 3. Typical $I-V_G$ transfer characteristic measured at 300 (a), 140 (b), 80 (c), and 8.5 K (d), respectively (with V_{SD} = 2 V for a−c; V_{SD} = 50 mV for d). A counterclockwise hysteresis loop occurs at room temperature (a) due to a charge−storage effect, while a competition between the ferroelectric effect and the charge−storage effect essentially closes the memory window at 140 K (b). At 80 K (c), a clockwise hysteresis loop is opened, indicative of a nonvolatile memory operation. At 8.5 K (d), a ferroelectric-modulated SET behavior is observed. The two red circles represent a bistable state. The sharp increase at a gate voltage of −6 V is due to leakage current.

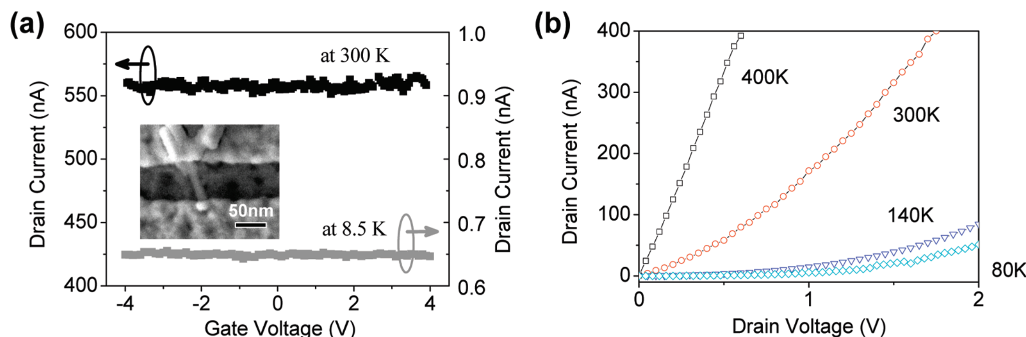

Figure 4. Typical transport measurements on an individual nanorod at different temperatures. (a) The transfer characteristics of a nanorod device shows negligible modulation, when sweeping back gate voltage from −4 to 4 V at both 300 K (at V_{SD} = 2 V) and 8.5 K (at V_{SD} = 50 mV). Inset: a SEM image of the measured arm (diameter 10 nm and length 60 nm) with the other two arms of the nanotetrapod buried underneath the electrode. (b) The corresponding temperature dependent $I-V$ curves of the nanorod measured at V_G = 0 V.

We now turn to discuss the origin of the field effect in CdS nanotetrapods. We first comparatively studied the electrical transport properties of the arm-only nanorod devices. As shown in Figure 4a, no obvious conductance modulation is observed in the nanorod alone at both 300 and 8.5 K. The same observation was confirmed in three tested devices. We did not see the Coulomb charging effect in any of the tested nanorod devices either, as demonstrated in $I-V_G$ curves shown in Figure 4a. Thus the observed field effect and Coulomb charging effect of the nanotetrapod both come from the arm/core/arm junction rather than from the arm itself. The lack of the field effect in the arm itself may be due to a surface screening effect (see Supporting Information for details) imposed by defects localized both on the surface and in the bulk of CdS arms.[41] As described in previous reports,[20,21] the growth processes of multi-armed CdS nanocrystals proceed in two steps: one is the fast nucleation of the tiny zinc-blend-structured core, and the other is the slow growth of the wurtzite-structured 1D arms via Ostwald ripening process. While the tiny cores usually have a well-crystallized "close-shell" structure, the relatively "long" arms formed afterward are much more prone to defects formation.

The temperature dependent conductance of the nanorod and the nanotetrapod devices are displayed in Figure 5a,b, respectively. An activated conductance can be seen for both devices, and the activation energies extracted from the Arrhenius fitting are ∼52 and

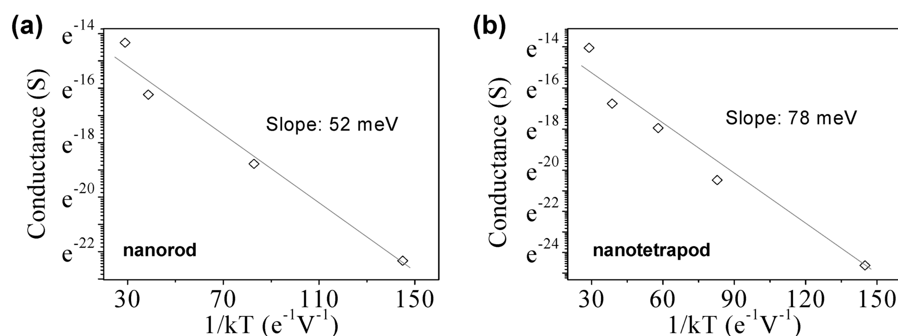

Figure 5. The temperature dependent conductance of the nanorod (a) and nanotetrapod (b) at V_{SD} = 0 V. Arrhenius fittings give rise to activation energies of ∼52 and ∼78 meV, respectively.

∼78 meV for nanorod and nanotetrapod devices, respectively. Namely, the activation energy of the nanorod device is significantly smaller than that for nanotetrapod. Measurements on five CdS devices give rise to a consistent value of 67−80 meV for nanotetrapod and 45−52 meV for nanorod, respectively. The energy barrier at the arm/core/arm junctions has been considered theoretically for CdX (X = S, Se, Te) nanotetrapod structures.[9−11,16] An energy barrier of 144 meV was calculated for electrons trapped at the core of CdSe nanotetrapod[8,9] which is in agreement with our extracted energy barrier of ∼78 meV for the CdS nanotetrapod. On the basis of these analyses, we can sketch a band diagram for the nanotetrapod (shown in Supporting Information Figure S3) with following essence. The Fermi level of the arm is pinned due to surface screen effect; however the Fermi level of the core can be tuned by the gate voltage. A negative (positive) gate voltage leads to smaller (larger) potential barrier at the arm/core interface and higher (lower) conductance, which gives a p-type transistor behavior in the nanotetrapod devices.

In summary, we have studied the electrical transport properties of individual CdS nanotetrapods with BST ferroelectric dielectric by using a four-probe STM. The ferroelectric film is found to enhance the gate capacitance coupling and thus give rise to a field effect modulation in nanotetrapods at room temperature. As a consequence of the nonvolatile memory effect of the ferroelectric gate dielectric, a proof-of-principle FeFET operation has been demonstrated in CdS nanotetrapods, with a SET behavior at 8.5 K. Furthermore, the conductance modulation is shown to originate from the arm/core/arm junctions of nanotetrapods, which can be rationalized by considering the type II band alignment at the zincblende core/wurtzite arm interface.

■ ASSOCIATED CONTENT

Supporting Information. Results on temperature dependent dielectric properties of both ferroelectric BST bulk and film (300 nm), the SET behavior of tetrapod transistors at 8.5 K, the calculation of electrostatic potential distribution inside the nanorod, and the scheme of the band offset of the nanotetrapod device. This material is available free of charge via the Internet at http://pubs.acs.org.

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