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Two-bit ferroelectric field-effect transistor memories assembled on individual nanotubes

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Abstract

Carbon nanotube (CNT) ferroelectric field-effect transistors (FeFETs) with well-defined memory switch behaviors are promising for nonvolatile, nondestructive read-out (NDRO) memory operation and ultralow power consumption. Here, we report two-bit CNT-FeFET memories by assembling two top gates on individual nanotubes coated with ferroelectric thin films. Each bit of the nanotube transistor memory exhibits a controllable memory switching behavior induced by the reversible remnant polarization of the ferroelectric films, and its NDRO operation is demonstrated. The low driving voltage of 2 V, high carrier mobility over 1000 $cm^2\ V^{-1}\ s^{-1}$, and potential ultrahigh integration density over 200 Gbit $inch^{-2}$ of the two-bit FeFET memory are highlighted in this paper.

1. Introduction

Due to its excellent electrical properties and nanometer-diameter, carbon nanotube (CNT) has been world-widely explored as one of the most promising candidates for creating the ubiquitous field-effect transistors (FETs) for next generation nanoelectronics [1–6]. On the other hand, ferroelectric oxide materials possessing a switchable and nonvolatile electric polarization can be applied as insulating layers, revealing new opportunities for use in devices for data storage [7–18]. In principle, the combination of the intrinsic memory functionality and the exceptional electrical properties of the nanotubes, may open a new route to nanoscale memory devices with ultrahigh integration density. Previously, back-gated nanotube (or nanowire) transistors with integrated ferroelectric dielectrics [19–25], have already been demonstrated to exhibit intriguing nonvolatile memory operation. In recent progress, we have reported a well-defined intrinsic memory switch behavior along with some of the most attractive performances of such a CNT ferroelectric FET (FeFET) memory unit [26]. An important next step would be the demonstration of its potential for high density and performance memory integration, which emphasizes the development of top (or local)-gate transistor devices with individual bias capability and also enhanced gate capacitance coupling.

Here, the nanotube is benignly coated with a ferroelectric thin film by using a 'two-step' pulsed laser deposition (PLD) method, based on which a CNT-FeFET memory with double-top-gates (acting as a series of two transistors) built on a single nanotube is realized, and its two-bit ferroelectric memory functions are demonstrated. Moreover, by using a biased atomic force microscopy (AFM) tip as a movable electrode to scan over the ferroelectric coated nanotube in a single line, we have achieved ferroelectric domain writing down to ∼50 nm, as confirmed by electric force microscopy (EFM) imaging, which is equivalent to an ultrahigh integration density over 200 Gbit $inch^{-2}$.

2. Experiments

A challenge for integrating CNT-FeFET memories comes from the fragility of CNTs when exposing them to an oxidizing environment at high temperature (600–800 °C) [27], which is required for '*in situ*' crystallization of ferroelectric thin films (PLD, for example). Here, we apply a 'two-step' PLD approach for benignly coating nanotubes with

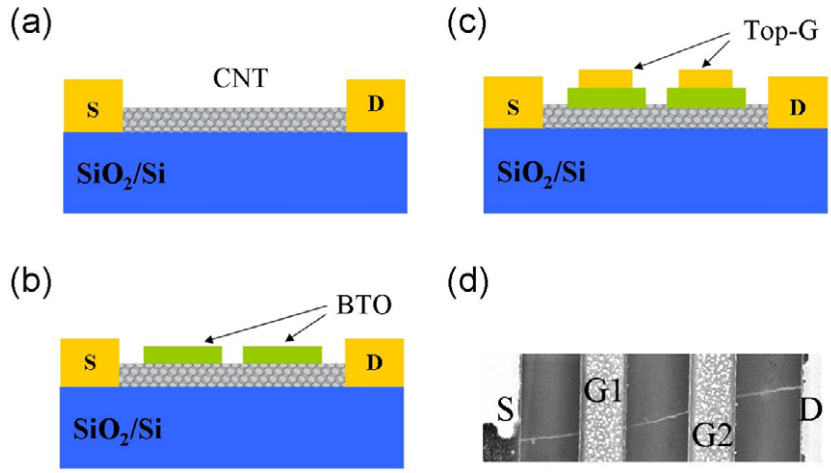

Figure 1. Scheme of the fabrication of the two top-gated FeFETs assembled on a single nanotube. (a) A CNT-FET fortuitously composed of an individual nanotube. (b) Coating of amorphous ferroelectric at room temperature onto the top of CNT-FET by using PLD. (c) After annealing, double top electrodes (G1 and G2) made of Pt were patterned in series onto the deposited ferroelectric films. (d) SEM image of the double-top-gated CNT-FeFET memory.

ferroelectric film. Conventional ceramic processing was used to prepare the $BaTiO_3$ ceramic disk-type targets with a density higher than 97% of the theoretical density. First, a 308 nm XeCl excimer laser, with reduced laser energy density of about 0.6 J cm^{-2}, was used to ablate the ceramic targets and deposit amorphous $BaTiO_3$ thin film at room temperature, then rapid post-annealing (RPA) in nitrogen gas at 600 °C for 5 min was applied to crystallize the ferroelectric films at the second stage. The CNTs used in this work were synthesized by patterned chemical vapor deposition (CVD) growth on SiO_2/Si substrates using 1–2 nm thick Fe thin films as catalyst islands. Electron beam lithography (EBL) was applied to pattern source (S) and drain (D) electrode pads made of Pd(5 nm)/Pt(80 nm) on the selected individual nanotubes to ensure both ohmic contact and good high-temperature sustainability. $BaTiO_3$ pads and the following Pt top electrodes were also patterned by using multi-step EBL processing. Transport measurements were performed using a B1500A semiconductor analyzer in dry air and at room temperature.

In addition, a metallized AFM tip was used to polarize the ferroelectric by applying a voltage between the AFM tip and the substrate as the tip was scanned over the ferroelectric coated nanotube in a single line, which was fabricated on another chip with the same ferroelectric coating and device fabrication process as described above. EFM was then applied for nondestructive probing of the local polarized domains. The EFM measurements were performed at a tip bias $V_{EFM} = -2$ V and a tip-to-surface distance $z = 50$ nm.

3. Results and discussion

3.1. Construction of two-bit CNT-FeFET

As shown schematically in figures 1(a) and (b), a 35 nm thick (measured by AFM) amorphous $BaTiO_3$ pad is firstly deliberately coated at room temperature with 1 Pa oxygen pressure on top of CNT-FET, which is fortuitously composed of an individual CNT synthesized by patterned CVD growth on SiO_2/Si substrates (as back gate). Secondly, the chip is rapidly annealed in pure nitrogen gas at 600 °C for 5 min, thus a crystalline ferroelectric is obtained while conserving the nanotubes at the same time. A 308 nm XeCl excimer laser with a reduced laser energy density of ∼0.6 J cm^{-2} (instead of the usual ∼2 J cm^{-2}) is used to ablate the ferroelectric $BaTiO_3$ ceramic targets, in order to minimize the sputtering energy of the evaporated particles that might destroy the structure of the ultrathin nanotube during deposition. Double top electrodes (G1 and G2) made of Pt are then patterned in series onto the ferroelectric pad (between the S and D electrodes) for the transistor (figures 1(c) and (d)). X-ray diffraction (XRD) patterns and AFM imaging of the as-annealed $BaTiO_3$ film confirm that it has crystallized into the perovskite phase with a condensed structure and smooth surface (figure 2).

3.2. Transfer characteristics of the CNT-FeFET device

Figure 3 shows typical current (I_D) versus gate voltage (V_G) characteristics ($V_D = 10$ mV) evolution of the CNT-FeFET before (inset black circle) and after (blue triangle) the fabrication of the Pt/ferroelectric gate stacks (for simplification, G1 and G2 were connected during this test). Obviously, the magnitude of the on-state current (e.g. at $V_G = 0$ V) of the top-gated transistor is at the same order compared with its back-gated counterpart that did not undergo ferroelectric coating. Its operation voltage has been greatly reduced from 40 V to less than 2 V, which is a significant advantage for realizing low power operation. The effective carrier mobility of the ferroelectric coated nanotube can be deduced as over 1000 cm^2 V^{-1} s^{-1} [26], indicating its promise for transistors. For this study, more than twenty transistors have been fabricated, which show similar results. These observations indicate that the ferroelectric films deposited on top of nanotubes are benign and the nanotubes were not destroyed during the processing. Because no high density

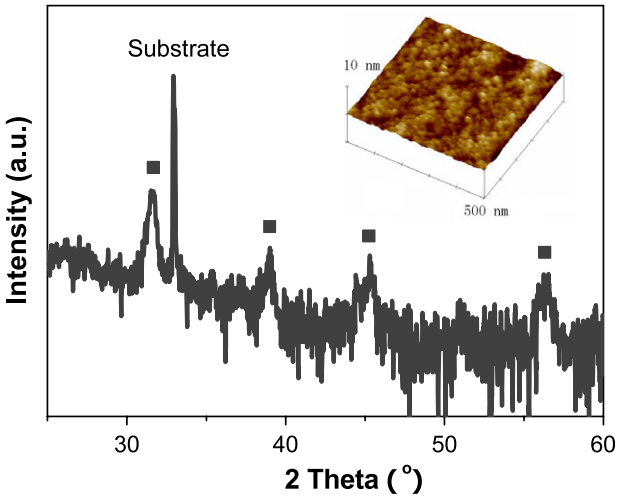

Figure 2. XRD pattern of the as-annealed ferroelectric $BaTiO_3$ deposited on the SiO_2/Si substrate and (inside) AFM image taken from a 0.5 μm × 0.5 μm area.

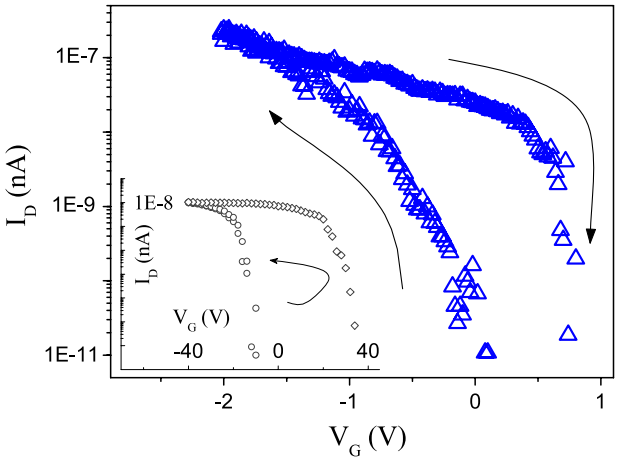

Figure 3. The transfer characteristics of the CNT-FeFET memory with a clockwise hysteresis loop. The clockwise hysteresis loop of transfer characteristics of the top-gated CNT-FeFET memory demonstrates the intrinsic ferroelectric behavior. The inset shows the I–V curve of the CNT-FeFET with SiO_2 back gate before ferroelectric film coating.

of scattering sites was introduced, the on-state current and carrier mobility were not obviously reduced. As a comparison, we carried out '*in situ*' coating of $BaTiO_3$ onto a nanotube transistor by using PLD at 600 °C with 1 Pa oxygen pressure. The device test showed that the nanotube transistor became electrically insulating after the coating, indicating the nanotube was destroyed. So the benign coating of nanotubes by ferroelectric films is important for this study.

In previous reports, conventional CNT-FETs could be used as memory devices due to the 'charge-storage' effect [28, 29], which exhibits a counter-clockwise hysteresis loop in the transfer characteristics for the p-type nanotubes. We first fabricated the device by using a conventional SiO_2 layer as the back gate, the transfer characteristics behave as a counter-clockwise hysteresis loop too, as shown in the inset of figure 3. In this study, the top-gated devices were constructed by using ferroelectric gates ($BaTiO_3$ films). The device tests show that the transfer characteristics of the FeFET is stamped by a clockwise hysteresis loop when the gate voltage (G1/G2) sweeps upwards (from negative to positive) and downwards continuously. The threshold voltage (V_{th}, defined as the gate voltage at which the CNT channel begins to conduct, e.g. I_D = 1 nA) has changed from 0.6 to −0.5 V as the gate voltage sweeps upward and downward, giving a large memory window ΔV_{th} of 1.1 V. Such clockwise hysteresis loops of the CNT-FeFETs are in agreement with the intrinsic memory operation induced by the ferroelectric films as expected [19, 20, 25, 26], which play a dominant role over the charge-storage memory effect. Although possible water molecule charge traps are not avoided, the charge-storage effect has been minimized by pre-baking the device at 180 °C for 4 h, and it has been suppressed to a large extent. Actually, if the top gate voltage is scanned between −1 and 1 V, which is within the range of the coercive voltage of the ferroelectric thin films (about ±2 V), no obvious hysteresis loop is detected in the transfer characteristics of the CNT-FeFET.

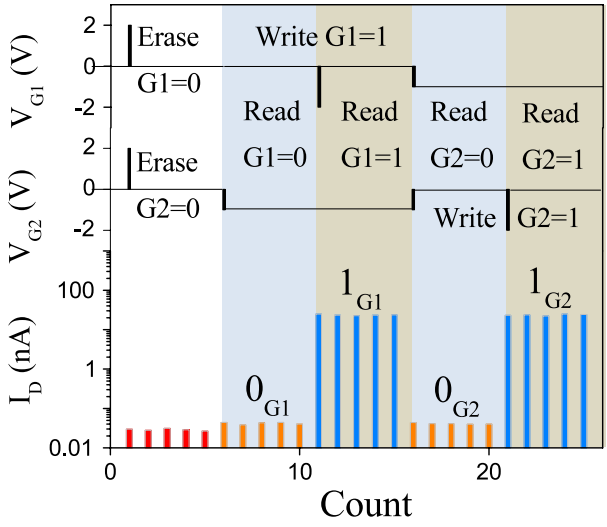

Figure 4. The schematic sequential chart for G1/G2 and the programming of the two top-gated CNT-FeFET memory.

3.3. Memory performances of two-bit CNT-FeFET memory

The above systematic transport measurements and analysis unambiguously reveal that both the memory functionality of the ferroelectric and the electrical properties of the nanotubes are retained well for the integrated CNT-FeFET memory. With respect to its memory operation, the above mentioned clockwise hysteresis loop is fundamental, that is, the modulation of the threshold voltages by the stored dipole moments in the ferroelectric film would lead to discriminated drain currents of each logic switch state in a memory [26], which enables two bits to be stored in the two-top-gate CNT-FeFET.

As shown in figure 4, the two-top-gate transistor memory is initially erased by applying a positive gate voltage of +2 V to both G1 and G2. This results in a 'turn off' of the flowing current in CNT (with a drain voltage V_D = 10 mV between

the S and D of the 12 μm-long CNT). Afterward, repeated reading of a specific transistor memory (e.g. G1 in figure 1(d)) is performed. For G2, a negative voltage smaller than the low threshold voltage (-0.5 V) of the transistor (but not enough to induce a polarization in the ferroelectric film), is applied (e.g. -1 V). As a result, independently of the 0/1 state, transistor G2 is switched on. Then, by applying a gate voltage to G1 with a value between the low and high (0.6 V) threshold voltages of the transistor memory (e.g. 0 V), we can now detect the nonvolatile logic state stored in the G1 transistor memory by simply reading the drain current. It is shown as '0_{G1}' or '1_{G1}' state (one bit) with reading drain currents of $\sim$0.04 and $\sim$20 nA in figure 4, separately, which is switched with a write gate voltage (with 0.1 ms pulse width) of -2 V ($V_D = 10$ mV). The reading procedure of each state is repeated five times with a time interval of 1 min. Since the positive or negative voltage pulses induce an upwards or downwards remnant polarization state of the ferroelectric thin films in configurations ($0_{G1}0_{G2}$, $1_{G1}0_{G2}$), we have in fact retentively and nondestructively read-out (NDRO) the remnant polarization and thus the bi-stable states of the G1 ferroelectric transistor memory via reading its drain current. It is noted that the small negative voltage -1 V (smaller than the coercive voltage of the ferroelectric thin film, so as not to change the polarization state of the ferroelectric film) is used to switch on another memory cell (independently of its 0/1 state), but it does not change its state.

The same operations are performed for G2. Repeating drain current readings both before and after memory switching from state '0_{G2}' to '1_{G2}' in configurations ($1_{G1}0_{G2}$, $1_{G1}1_{G2}$) are shown in figure 4. Thus, we have demonstrated writing and reading two bits together in configurations ($0_{G1}0_{G2}$, $1_{G1}0_{G2}$, $1_{G1}1_{G2}$), as well as the configuration $0_{G1}1_{G2}$. Therefore, by demonstrating the bi-stable state switching and NDRO operation of both G1 and G2 transistor memory in configurations ($0_{G1}0_{G2}$, $1_{G1}0_{G2}$, $0_{G1}1_{G2}$, $1_{G1}1_{G2}$), the basic memory functions of the two-bit CNT-FeFET are fulfilled.

3.4. Demonstration of potential high density

Other advantages of the CNT-FeFET memory cell include its simple one-transistor (1T) structure (a cell size of $4F^2$) and the small size ($\sim$1 nm diameter) of the nanotubes that surpass the structure attainable by top-down lithography ($\sim$10 nm), both of which are essential to miniaturization. We show here that, by using a biased AFM tip as a movable electrode to scan over the nanotube coated with ferroelectric film, the current through the nanotube can be tuned. The single line scan was carried out at an AFM tip voltage $V_{tip} = +5$ V with the tip gently contacting the ferroelectric film. A slow scanning rate of 20 nm s^{-1} was used. As shown in figure 5, more then a ten fold reduction of the drain current between the 'on' and 'off' state of the nanotube transistor memory was observed before (empty red diamond) and after (empty blue diamond) AFM scanning (white dashed line). Next, EFM was applied for nondestructively probing the local polarized domains before (rectangle with red edge) and one day after (blue edged rectangle) the scanning. It revealed that we had achieved ferroelectric domain writing down to $\sim$50 nm located at the crossing points of the single AFM scan line and the two nanotubes (dashed blue circle). This is equivalent to a significant integration density over 200 Gbit inch^{-2}, even though the above tests were performed without optimization.

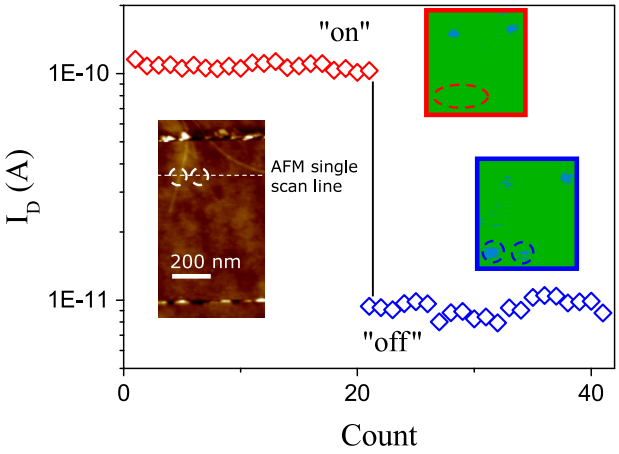

Figure 5. Ferroelectric domain writing by using a biased metallized AFM tip as movable electrode. More than a ten fold reduction of the current between the 'on' and 'off' state of the memory device was observed before (empty red diamond) and after (empty blue diamond) single line scanning (white dashed line), which was carried out at $V_{tip} = +5$ V by gently contacting to the ferroelectric thin film with a slow scanning rate of 20 nm s^{-1}. *Left inset*, the biased AFM tip first scanned over the two nanotubes along a single line to polarize the ferroelectric film. *Right inset*, EFM was applied for nondestructive probing of the local polarized domains before (rectangle with red edge) and one day after (rectangle with blue edge) scanning. Polarized domains around 50 nm located at the crossing points of the AFM scan line and the two nanotubes (white dashed circle) were confirmed (dashed blue circle), which corresponds to an integration density of $\sim$200 Gbit inch^{-2}.

4. Conclusion

In summary, by using a 'two-step' PLD method, we have achieved the benign integration of ferroelectrics into CNT transistors, based on which two-bit FeFET memories have been fabricated on individual CNTs, and their controlled switching, NDRO memory operation, and high carrier mobility $\sim 10^3$ cm^2 V^{-1} s^{-1} along with potential integration density over 200 Gbit inch^{-2}, are demonstrated. These results represent new progress in harvesting both the memory functionality of the ferroelectrics and the exceptional properties of perfect nanotubes for nanoscale memory applications.

Acknowledgments

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