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Medium-scale flexible integrated circuits based on 2D semiconductors

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Two-dimensional (2D) semiconductors, combining remarkable electrical properties and mechanical flexibility, offer fascinating opportunities for flexible integrated circuits (ICs). Despite notable progress, so far the showcased 2D flexible ICs have been constrained to basic logic gates and ring oscillators with a maximum integration scale of a few thin film transistors (TFTs), creating a significant disparity in terms of circuit scale and functionality. Here, we demonstrate medium-scale flexible ICs integrating both combinational and sequential elements based on 2D molybdenum disulfide (MoS_2). By co-optimization of the fabrication processes, flexible MoS_2 TFTs with high device yield and homogeneity are implemented, as well as flexible NMOS inverters with robust rail-to-rail operation. Further, typical IC modules, such as NAND, XOR, half-adder and latch, are created on flexible substrates. Finally, a medium-scale flexible clock division module consisting of 112 MoS_2 TFTs is demonstrated based on an edge-triggered Flip-Flop circuit. Our work scales up 2D flexible ICs to medium-scale, showing promising developments for various applications, including internet of everything, health monitoring and implantable electronics.

Flexible electronics, integrating both electronic functionalities and mechanical flexibility, holds great promise for the transformation of human life with more comfort and convenience owing to a plethora of emerging technological innovations, including wearable/implantable devices, foldable smart terminals, bioinspired soft robotics and human-machine interfaces[1–3]. Specifically, multifunctional flexible integrated circuits (ICs), which facilitate the seamlessly information processing, interaction and integration with human beings, objects, and ambient environments, would strongly advance the era of internet of everything (IoE). Over the past decades, huge efforts have been devoted to fabricating flexible electronic devices based on organic semiconductors[4–6], indium gallium zinc oxide (IGZO)[7,8], carbon nanotubes (CNT)[9–11], and amorphous/polycrystalline silicon[12–14]. Although significant progress has been witnessed, the low carrier mobility, interfacial disorder, low yield, or the lack of device uniformity and reproducibility over large areas create critical roadblocks towards practical applications.

Remarkably, the emergent two-dimensional (2D) semiconductors with the unmatched combination of high electrical properties, mechanical flexibility and enhanced biocompatibility, introduce a promising avenue for the nascent flexible ICs[15]. The advantages of 2D flexible devices have largely been validated and agreed upon over the past few years, such as high-speed flexible electronics[16,17], high-performance ICs with low power consumption[18,19] and artificial

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retinas enabled by optoelectronics[20]. However, the demonstrated 2D flexible ICs have thus far been constrained to basic logic gates and ring oscillators, with a maximum integration scale of merely 24 thin film transistors (TFTs)[18]. This limited capability only enables to perform simple operations, leaving a significant gap towards cutting-edge applications in terms of circuit scale and functionality. To fully harness the potential of flexible 2D ICs, it is of the utmost importance to upgrade the TFT integration scale, and to implement multifunctional digital electronic systems integrating both combinational and sequential circuits in a single chip with hundreds to thousands of TFTs working collaboratively[21].

In this work, we demonstrate the medium-scale flexible ICs integrating more than 100 TFTs based on the 2D semiconductor MoS_2. An impedance modulation is employed to create both the enhancement-mode (E-mode) and depletion-mode (D-mode) transistors and further implement the NMOS inverters based on zero-V_{gs} load logic. The flexible MoS_2 transistors demonstrate good flexibility and uniformity. Additionally, our design ensures robust rail-to-rail operation with sufficient noise margin, which is crucial for ensuring the stable operation of various digital elements, making it an ideal standard cell for constructing medium-scale complex circuits. To this end, we demonstrate both combinational and sequential logic circuits, incorporating representative elements such as a half-adder, latch, flip-flop, and a medium-scale clock division module, offering potential applications in digital ICs and IoE system.

Results

Co-optimization of processes for medium-scale flexible MoS_2 ICs

The digital ICs constructed by a set of combinational and sequential logic elements sit at the heart of electronics systems, which are responsible for tasks such as data computation, signal processing, and control functions[15]. Figure 1a illustrates the inter-relationship between the combinational and sequential circuits within a register transfer level (RTL) abstraction[22]. Data signals are sent into the combinational logic (CL) block performed with specific logic operation and then captured by sequential elements (e.g., register) for temporary storage. Under the regulation of the clock signal, the data will soon propagate from this register to the next one in a synchronized manner, enabling time-dependent operations.

2D semiconductors such as MoS_2 with atomic thicknesses and dangling-bond-free flat surface not only hold great promise for further scaling ICs to the end of roadmap, but also offer extraordinary opportunities for the nascent flexible nanotechnology because of their superior mechanical flexibility afforded by their atomically thin nature[23]. To transcend the current integration scale and implement flexible 2D ICs with comprehensive functionalities, it requires the co-optimization of technology processes to achieve reliable batch fabrication of flexible 2D TFTs with high yield and low device-to-device variations. To realize this long-sought goal, we optimize every step of technical process (Fig. 1b and Supplementary Fig. 1). (1) we employ the gate-first device architectures, which facilitate the deposition of high-quality high-κ dielectric layers. It is noteworthy that for the local metal-gate fabrication, a double-layer-photoresist technology is utilized, as presented in Supplementary Fig. 2, creating an undercut structure crucial for both high-yield lift-off and reduced edge burr of the gate pattern[24]. (2) We pre-deposit 20 nm HfO_2 on flexible poly ethylene terephthalate (PET) substrates as barrier layer before metal-gate deposition to reduce the surface roughness and protect the susceptible polymer substrates from solution-induced deformation (Supplementary Fig. 3), given that the double-layer-photoresist requires lift-off process in both organic and alkaline solutions. (3) we adopt a dual-transfer technology with a combination of wet and dry transfer processes (see Methods). Together with epitaxially grown high-quality 4-inch wafer-scale monolayer MoS_2 films which are characterized by rigorous layer uniformity and significant large grain size (Supplementary Fig. 4), the integrity of the MoS_2 thin films transferred onto the flexible substrates is significantly bolstered, facilitating flexible TFTs with high yield and uniformity. (4) Later upon the contact formation, we employ a *n*-doping technique involving sub-stoichiometric AlO_x capping layer on the load transistors[25]. This

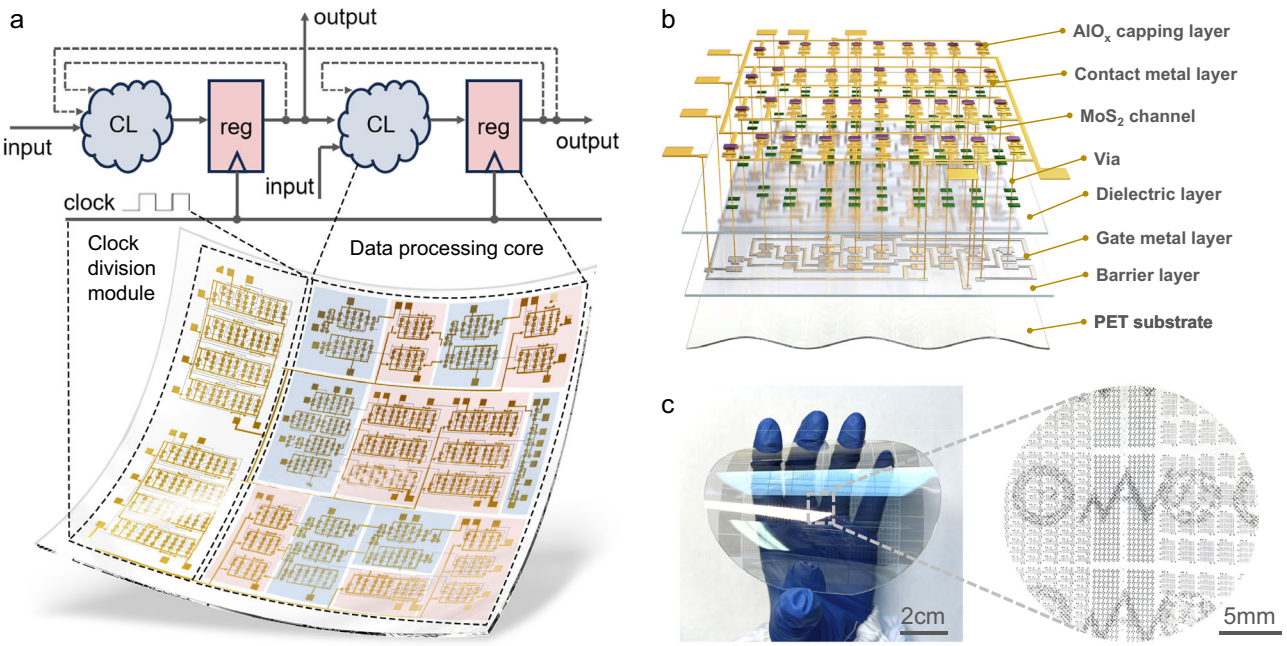

Fig. 1 | Co-optimization of processes for medium-scale flexible MoS_2 integrated circuits (ICs). a Schematic of flexible electronics incorporating both clock division module and data processing core in the internet of everything (IoE) paradigm. The upwards flow diagram demonstrates the inter-relationship between different blocks within register transfer level (RTL) abstraction, where CL: combinational logic, reg: register. **b** Detailed layer structure of the as-fabricated MoS_2 ICs on the flexible substrate. **c** MoS_2 flexible ICs fabricated on a 4-inch poly ethylene terephthalate (PET) substrate consisting both the combinational and sequential elements. The zoomed-in image showcases the representative circuit blocks including inverters, flip-flops and medium-scale clock division modules.

enables a robust rail-to-rail operation of the basic building blocks and further improves the stability of the medium-scale cascaded ICs which we shall come to shortly.

Therefore, the co-optimization strategy incorporates double-layer photoresist technology, pre-deposition of the HfO_2 barrier layer, utilization of monolayer MoS_2 for transistors, and doping with a sub-stoichiometric AlO_x capping layer. These enhancements collectively improve device performance, uniformity, and yield, thereby increasing the reliability and consistency of flexible transistor and IC fabrication.

Figure 1c shows the as-fabricated medium-scale MoS_2 ICs on a 4-inch transparent flexible PET substrate, including both combinational and sequential elements such as NAND/NOR gates, half adder, and flip-flops. The zoomed-in image shows the details of the representative positive-edge-triggered Flip-Flops (left), inverters (middle) and clock division modules (right). We highlight that the clock division module featured on this chip, consisting of 112 transistors, marks the inaugural demonstration of medium-scale flexible ICs based on 2D semiconductors.

Flexible MoS_2 TFTs

To verify the device flexibility of the afore-mentioned gate-first technology, we firstly fabricate array of flexible MoS_2 TFTs on PET substrates with channel lengths varying from 5 to 50 μm and channel widths ranging from 20 to 60 μm (Fig. 2a). Note that transistors based on bilayer MoS_2 obtained through the dual-transfer technology not only achieved improved device yield but also demonstrated enhanced performance metrics, including reduced variation, smaller subthreshold swing, and higher on-state current compared to those based on monolayer MoS_2, as shown in Supplementary Fig. 5. Consequently, we selected the bilayer MoS_2 technology for our device fabrication. Figure 2b presents the double sweep transfer curve of a typical bilayer MoS_2 device, demonstrating an high on/off ratio exceeding 10^8 and narrow hysteresis ΔV_g of ~120 mV (inset of Fig. 2b). The small hysteresis indicates a minimal impedance variation at a given voltage during a dynamic operation, which is crucial for constructing inverters and ICs with robust operations. The corresponding output curves are depicted in Fig. 2c, exhibiting a favorable linear behavior and thus indicating a good Ohmic contact.

In order to evaluate the device resilience against certain mechanical strain, we perform various tests in terms of both the bending radius and times. Figure 2d displays the transfer curves and leakage currents under different conditions. The corresponding tensile strain within the device is calculated according to the bending radius (R) and half of the film thickness (d) by $\varepsilon = d/R$[10], where $d = 0.12$ mm. Both the output and leakage currents demonstrate negligible performance degradation under the tensile strain of more than ~2%. The on-current seems remain visually unaltered up to 2% of strain. This contrasts with some previous studies show the enhancement of on-current of MoS_2 by strain engineering[26–29]. A possible origin of the almost unchanged on-current may be competition between the reducing of intervalley scattering trigged by strain and strain-induced degradation of device performance. It is noteworthy that although a slight shift of threshold voltage (V_{th}) is observed during bending, the resulting transfer curves still fall within the overall statistical distribution mentioned below. The observed shift in V_{th} can be attributed to several factors: polarization charges generated by mechanical strain affecting carrier distribution, the introduction of new defects and trap states that capture and release charge carriers, and altered Schottky contact characteristics, which change the electric field distribution in the contact region. Moreover, the devices exhibit high tolerance in a 10^3-cycle bending fatigue tests under the strain of 1.23% (Fig. 2e, f). Despite a slight degradation in the on/off ratio caused by the increase in off-state current, the critical parameters extracted throughout the test show no significant variations, highlighting resilient flexibility of the devices.

Basic building blocks with robust rail-to-rail operations

Aside from the good flexibility of the as-fabricated transistors, it is also crucial to achieve fundamental building blocks (e.g., inverters) with

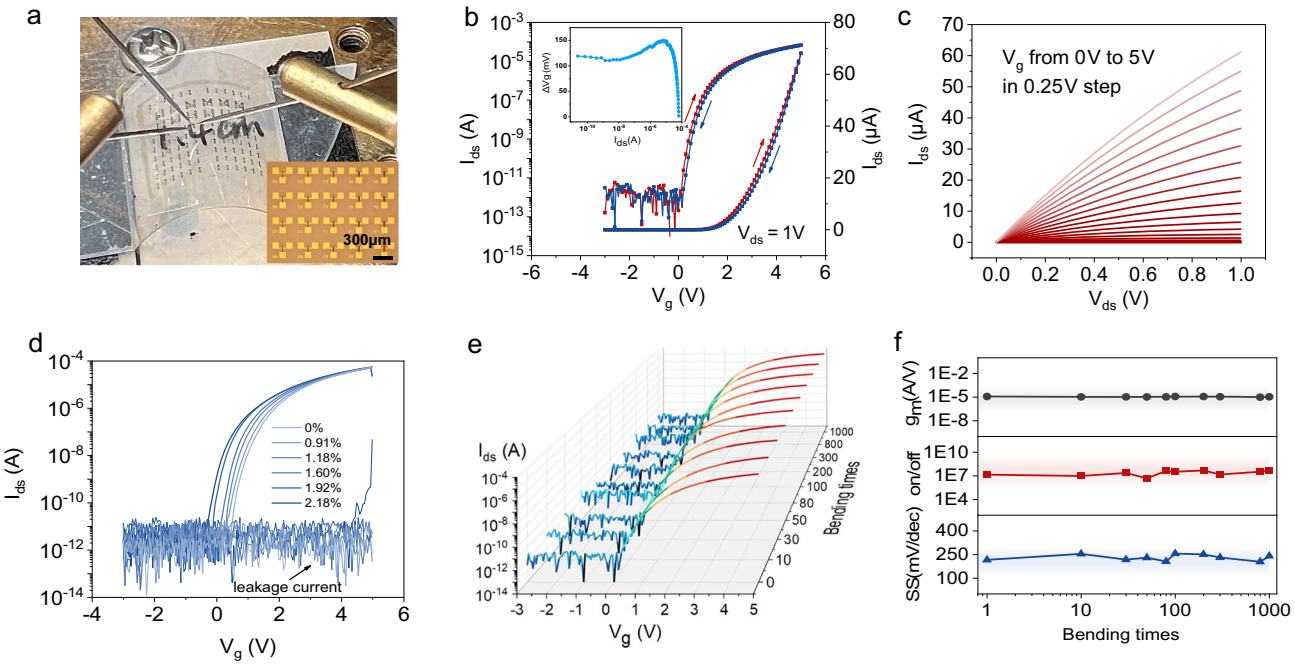

Fig. 2 | Flexible MoS_2 transistors. a The measurement setup for the bended devices and the inset shows an array of flexible MoS_2 thin film transistors (TFTs) on PET substrate with different channel length and width configurations. **b** The double transfer curves of a typical device (L = 10 μm, W = 40 μm). Inset: the hysteresis widths across the entire I_{ds} range. V_{ds}: the source-drain voltage, I_{ds}: the source-drain current, V_g: the back-gate voltage, where ΔV_g is the difference of back-gate voltage at the same I_{ds}. **c** Output curves of the same device in (**b**) exhibiting Ohmic behavior. **d** Transfer curves of flexible MoS_2 TFTs with different strains. **e** Transfer curves of a device throughout a set of bending fatigue test up to 1000 times. **f** Corresponding parameters extracted from (**e**) for evaluating device performance variations, where g_m is the transconductance, on/off: on/off ratio, SS: the subthreshold swing.

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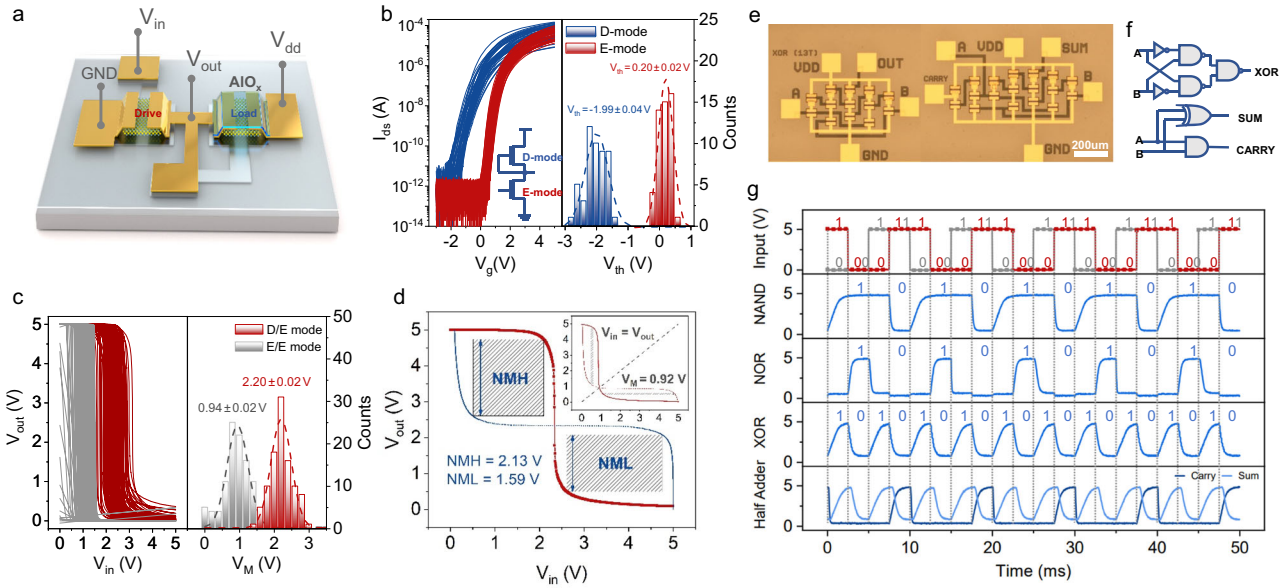

Fig. 3 | Basic building blocks with robust rail-to-rail operations. a Schematically illustration of MoS_2-based NMOS inverter with AlO_x capping layer on the load transistor. NMOS N-Metal-Oxide-Semiconductor, V_{in} the input voltage, V_{out} the output voltage, V_{dd} drain voltage. **b** Transfer curves and the corresponding statistic results of V_{th} for 100 E-mode and D-mode transistors, the dashed line represents the fitted normal distribution curves. Inset: circuit diagram of NMOS inverter based on zero-V_{gs} load logic. V_{th}: the threshold voltage, E-mode: enhancement-mode, D-mode: depletion-mode. **c** Voltage transfer characteristics and the corresponding midpoint voltages (V_M) of 100 D/E mode and 100 E/E mode inverters, and the dashed line represents the fitted normal distribution curves. **d** Noise margin comparison of the inverters with and without (inset) the intentional doping technique, NMH: noise margin high, NML noise margin low. Optical image (**e**) and corresponding circuits diagram (**f**) of the flexible MoS_2-based XOR and half-adder circuits. **g** Dynamic measurements of the NAND, NOR, XOR, and half-adder circuits with V_{dd} = 5 V.

robust rail-to-rail operations, allowing to maintain logic integrity when cascading into medium-scale ICs. In order to construct MoS_2-based NMOS rail-to-rail inverters with sufficient noise margin, we employ an intentional doping technology with a sub-stoichiometric AlO_x capping layer on the load transistor (Fig. 3a). The oxygen vacancies in the sub-stochiometric AlO_x induce electron doping in the conduction band of MoS_2, and thus cause a negative V_{th} shift in the load transistor (Fig. 3b and Supplementary Figs. 6, 7), thereby effectively transforming E-mode into a D-mode transistor[30]. This strategic modulation of the load transistor, operating as a current source in zero-V_{gs} mode, aligns its resistance comparable with the drive transistor under a specified input voltage, allowing for precise manipulation of the switching threshold voltage towards statically-ideal $V_{dd}/2$ in the inverters and leading to enhanced robustness in cascade ICs. In order to evaluate the device uniformity before and after doping, we measure 100 randomly picked as-fabricated D-mode and E-mode transistors on flexible PET substrates. The statistical transfer curves and their corresponding V_{th} are shown in Fig. 3b. The standard deviations are of ~10%, comparable with the state-of-the-art results of the well-developed flexible TFT technology based on CNTs or 2D devices on rigid substrates[21,31]. The overall high uniformity and reliability allow to optimize the standard inverter cells in terms of their performance, stability, and noise immunity, promising the prospect for scaling up 2D flexible ICs to medium-scale with comprehensive functionality and desired performance. The statistic voltage transfer characteristics (VTC) of 200 inverters in E/E mode and D/E mode are shown in Fig. 3c. The D/E mode inverters shift their switching threshold voltage to ~2.2 V, whereas inverters with identical transistor design achieve a tripping point of ~0.94 V. This tight distribution of D/E mode inverters with reliable rail-to-rail operation confirms the dependability of this design configuration for cascading multiple logic stages. Besides, as shown in Fig. 3d and Supplementary Fig. 8, the VTC of D/E mode inverter demonstrates stable logic low and high values with negligible voltage loss, and the corresponding noise margin is highly symmetrical and adequate with 2.13 V noise margin high (NMH) and 1.59 V noise margin low (NML). Please see Supplementary Figs. 9 and 10 for more characteristics of the D/E mode inverter. Next, we verify the logic operations of the basic logic gates, which serve as the foundation for implementing any combinational circuits. Figure 3e, f show respectively the optical image and the corresponding circuit schematics of the representative XOR and half-adder. For the XOR gate implementation, a 13-transistor[32] instead of 9-transistor[33] configuration is utilized, ensuring a balanced pull-up and pull-down network, thereby reducing skew difference between the rising and falling edges. Figure 3g presents the dynamic measurements of the NAND, NOR, XOR, and half-adder circuits. A pair of synchronized pulses, comprising all possible combinations of "0" and "1", are used as the input signals. The corresponding circuits demonstrate accurate Boolean functions and ideal rail-to-rail operation in response to the input signals, please see Supplementary Fig. 11 for more characteristics. The half-adder circuit, responsible for adding two binary digits, provides a preliminary demonstration of common combinational circuits. These foundational elements lay the groundwork for implementing various combinational circuits, such as an arithmetic logic unit (ALU) that serves as a crucial component of a microprocessor[4,34].

Sequential circuits and medium-scale flexible module

The combinational circuits, generate outputs based independently on the current inputs. Another type of circuit is sequential circuits in which the next outputs not only depend on the current inputs but also rely on the current state of the circuit. This kind of circuits possess the capability to store and maintain the circuit's state, and is essential for controlling the data flow on the signal processing path. Here, we demonstrate the basic memory elements, latch and flip-flop circuits, all of which are commonly utilized for storing 1-bit binary signals. The corresponding circuit diagrams are depicted in Fig. 4a. By incorporating a feedback loop, these circuits enable latching onto a specific state and retaining it until a new input is received. Additionally, the

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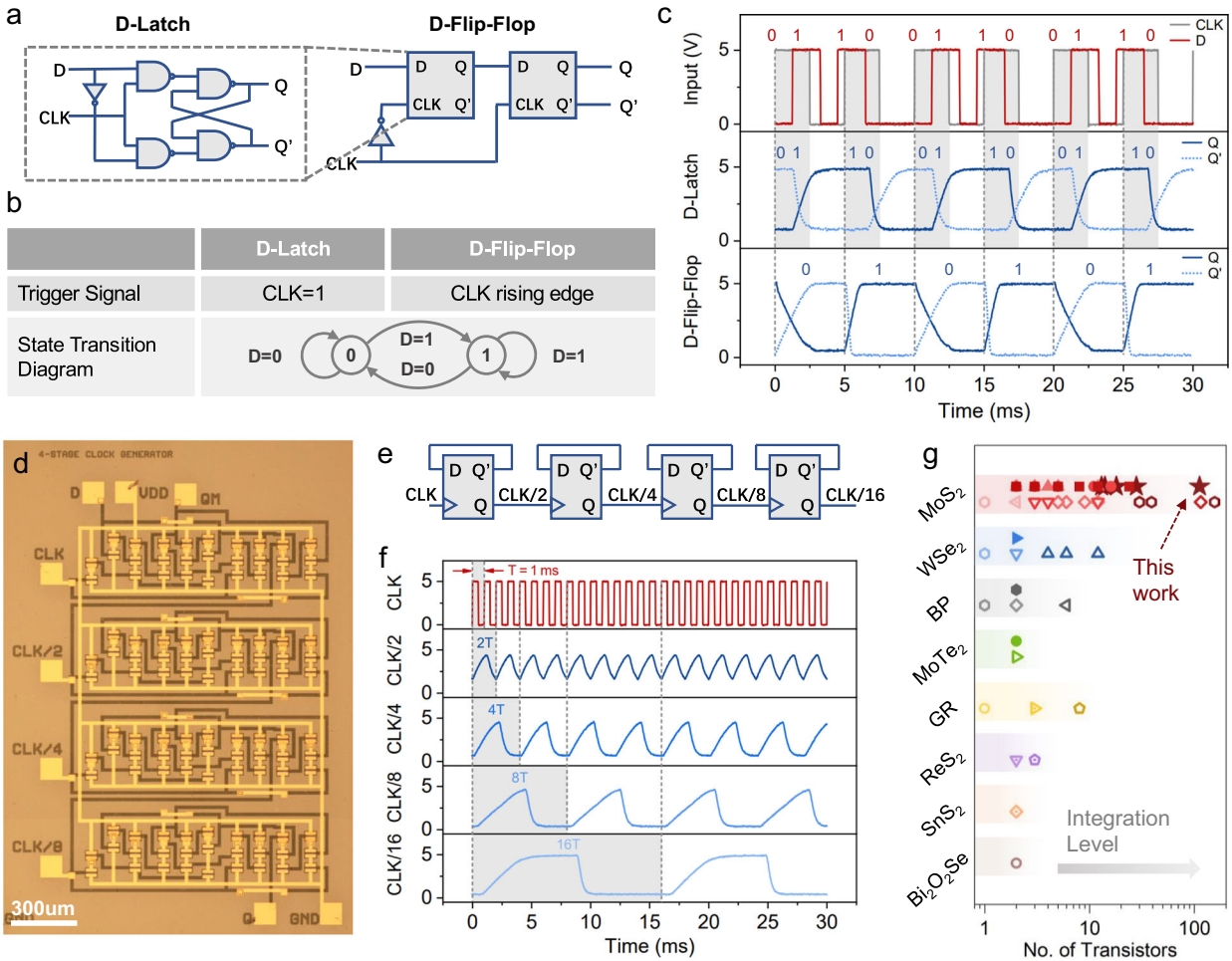

Fig. 4 | Sequential circuits and medium-scale module based on flexible MoS_2 transistors. a Circuit diagrams of the D-Latch and D-Flip-Flop circuits. **b** The trigger condition and corresponding state transition diagram of the sequential elements. Note that the current state (Q) is a function of both the input signal (D) and previous state. **c** Output characteristics of the D-Latch and D-Flip-Flop circuits. The gray shadow and dashed line indicate the period when the sequential elements are sensitive to the input signals. **d** Optical image of a flexible MoS_2-based clock division module consisting of 112 transistors. **e** The medium-scale clock division module constructed by 4 toggled flip-flop dividers. **f** Measured waveform of the clock division module with a 1 kHz input clock rate. **g** Benchmark of the integration level of ICs implemented with 2D materials[36–52]. The solid (hollow) symbol represents the flexible (rigid) 2D ICs.

circuit's state can also be set to "0" or "1" based on the trigger signals. The trigger condition of the circuit and its related state transition diagram are illustrated in Fig. 4b. Figure 4c shows the measured waveform for the D-Latch. The output state Q follows the input signal D when the clock signal is at high value (indicated by the gray shade area), and the final state of Q will be latched into a stable value when the clock changes to low. Note that the latch circuit is voltage level-sensitive, i.e., in the period of CLK = 1 any changes in D will cause flip of state in Q, resulting a diminished resistance to interference. In order to enhance the reliability and prevent undesired state change, we also constructed the edge-triggered Flip-Flop based on the D-Latch in the master-slave configuration[35]. The resulting D-Flip-Flop exhibits state reversal only at the rising edge of the clock signal (indicated by the dashed line) and remains undisturbed throughout the rest of the period (Fig. 4c). We highlight that the realization of flexible sequential circuits based on 2D semiconductors is essential for forming a complete data path with the combinational elements.

Based on the edge-triggered Flip-Flop, we also fabricate a clock division module (also worked as a hexadecimal counter) on the flexible PET substrate. Importantly, this module incorporates 112 MoS_2 transistors, yielding a medium-scale 2D ICs (Fig. 4d). The implementation of the circuit is shown in Fig. 4e. The toggle flip-flop dividers are connected in series, forming an asynchronous sequential circuit[8]. The functionality of the clock division module, tested with a 1 kHz input clock rate, demonstrates the generation of accurate frequency clock signal at each node and maintains stable operation before and after bending, as shown in Fig. 4f and Supplementary Fig. 12. Notably, when comparing the results before and after bending, both delay and output swing show improvements, albeit with an increase in power consumption. Following bending, the output waveform and overall performance demonstrate slight enhancements, likely attributable to the shift in the device's threshold voltage induced by the applied stress. A lower V_{th} may facilitate quicker device activation, thereby reducing delay times and stabilizing output waveforms. This shift can enhance dynamic response, resulting in a favorable trade-off between speed and power efficiency. Additionally, this clock division module could be responsible for generating separate clock signals based on the requirements of different submodules within a single chip. For practical applications, improvements can be made by minimizing parasitic capacitance through the use of materials with lower dielectric constants and reducing the number of vias, adjusting the threshold voltage of the transistors, and enhancing the quality of the MoS_2 material and fabrication process to improve circuit performance and switching speed.

Finally, for evaluating the integration level of 2D ICs, we benchmark our results with other commonly used 2D materials, including

WSe_2[36–39], Black Phosphoros (BP)[37,40–42], $MoTe_2$[43–45], Graphene (GR)[46–48], ReS_2[49,50], SnS_2[51] and Bi_2O_2Se[52] (Fig. 4g). Among these, MoS_2 ICs are the most well-developed both on rigid[30,32,34,53,54] and flexible[18,19,55] substrates, exhibiting the highest level of integration. Note that this work showcases the demonstration of medium-scale flexible 2D ICs, incorporating more than 100 transistors and enabling both combinational and sequential logic functions. Leveraging our co-optimization of circuit fabrication technology, the integration capacity of the flexible MoS_2 ICs has advanced to medium-scale scalability, being on the same level of 2D rigid ICs. Our results fully exemplify the potential of 2D materials in flexible ICs applications, demonstrating their promising prospects for maintaining high performance and yield when further down-scaling the size and increasing the scale of integration. Furthermore, future research may leverage the direct growth of TMDs on flexible substrates, which has been shown to improve device yield, reliability, and interface quality compared to traditional processes[56,57].

Discussion

Medium-scale flexible ICs based on MoS_2 TFTs are successfully realized by co-optimizing the fabrication technology. Additionally, the implementation of the AlO_x doping technique and the zero-V_{gs} load logic configuration enables robust rail-to-rail operation of the inverters, establishing a solid foundation for constructing reliable medium-scale circuits. Remarkably, both the combinational and sequential circuits with correct logic functions are demonstrated, and can be further integrated into functional circuit blocks capable of executing specific instructions. This work scales up the 2D flexible ICs to the medium-scale, representing an important advancement toward various practical applications, such as wearable electronics, foldable smart terminals, and IoE applications.

Methods

Growth of 4-inch MoS_2

The growth of monolayer MoS_2 is performed in a homemade 3-temperature zone CVD system. Pre-annealed 4-inch sapphire (0001) wafers are placed in the 3rd zone of the furnace as substrates and sulfur (Alfa Aesar, 99.9%, 20 g) and MoO_3 (Alfa Aesar, 99.9%, 240 mg) powder loaded in separate quartz tubes are placed in the 1st and 2nd zone, respectively, as the reaction sources. In a typical growth, the reactive sulfur and MoO_3 are carried with 40 sccm Ar and 240 sccm Ar/8 sccm O_2 gas respectively to the substrate for epitaxy. The temperatures are kept at 160 °C (1st zone), 580 °C (2nd zone), and 930 °C (3rd zone) and the system pressure is ~1 Torr. For the full coverage of a 4-inch substrate, the epitaxial growth typically lasts for 45 min.

Fabrication of flexible MoS_2 ICs

The PET thin film is attached to a supportive rigid substrate, baked at 110 °C for one hour on a hot plate, and then pre-deposited with 20 nm HfO_2 as the barrier layer, preventing the deformation and delamination of the flexible substrates throughout the entire fabrication process. The substrate is spin-coated with LOR 5 A (Microchem)/AZ6130 bilayer-photoresist, and then exposed by direct-write laser lithography (DWL 66+), enabling the gate patterns with undercut structures. Ti(2 nm)/Au(8 nm)/Ti(2 nm) is deposited by e-beam evaporation system and followed with lift-off process in acetone and AZ 300MIF successively. After O_2 plasma treatment for surface cleaning, 30 nm HfO_2 is deposited globally as dielectric layer by ALD (KE-MICRO TALD-150D) using Tetrakis(dimethylamido)hafnium(IV) and H_2O as precursors. The dual-transfer of MoS_2 is carried out by both wet and dry transfer method starting with MoS_2/sapphire spin-coated with 5% 950 polymethyl methacrylate (PMMA). For the wet-transfer, the PMMA/MoS_2/sapphire stack is etched in KOH solution for 40 min, and then peeled off and picked up in water by the target substrate. The dry-transfer is aided with a thermal releasing tape (TRT), which could directly peel off the stack from sapphire substrate and transfer onto the target substrate without picking up the floated MoS_2 film from water. This could effectively prevent the first layer of MoS_2 on target substrate from delamination under water when picking up the second one. Reactive ion etching (PlasmaPro NGP80 RIE, Oxford Instruments) is implemented for both of the channel definition and via formation using O_2 plasma and SF_6/Ar plasma respectively. Finally, Au(2 nm)/Ti(2 nm)/Au(30 nm) is deposited and lift-off in achieving the contact formation.

Optical and electrical measurements

The photoluminescence (PL) and Raman spectra are acquired using a JY Horiba HR800 system with a laser wavelength of 532 nm at room temperature. The electrical measurements are carried out in a vacuum probe station (Janis) with a semiconductor parameter analyzer (Agilent B1500) and a digital oscilloscope (Agilent DSO-X 3054 A). The waveforms of the digital elements are captured by the oscilloscope, which is connected to a 100 MΩ resistor for signal amplification, and had an input impedance of 1 MΩ.

Data availability

Relevant data supporting the key findings of this study are available within the article and the Supplementary Information file. All raw data generated during the current study are available from the corresponding authors upon request.

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G.Z. supervised the project. L.L., Q.W., and Y.Z. performed the epitaxial growth of the 4-inch MoS_2. Y.P. fabricated the flexible circuits with help from C.C., Y.W., J.Ti., B.H., J.Ta., X.L. Y.P., and C.C. performed the electrical measurements with help from J.Ti., Z.H. and Y.C. Y.P., N.L., L.D., W.Y., D.S. and G.Z. analyzed data. Y.P., N.L., L.D., and G.Z. wrote the manuscript and all authors commented on the manuscript.

Competing interests
The authors declare no competing interests.

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